AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (previously presented) A method for programming non-volatile memory, comprising:

categorizing particular non-volatile storage elements in a set of non-volatile storage elements into three or more different groups, each particular non-volatile storage element being categorized into one of the different groups based on its detected behavior; and

programming said particular non-volatile storage elements using a different programming condition for each of the different groups.

2. (previously presented) The method according to claim 1, wherein:

said step of programming includes applying different bit line voltages for the different groups.

3. (previously presented) The method according to claim 1, wherein:

said step of programming includes applying a program voltage to said particular non-volatile storage elements via a common word line and applying different bit line voltages for the different groups.

4. (previously presented) The method according to claim 1, wherein:

said step of categorizing includes determining relative programming speeds of said particular non-volatile storage elements, each of the different groups including particular non-volatile storage elements with similar relative programming speeds.

5. (previously presented) The method according to claim 1, wherein:

said step of categorizing includes determining programmability of said particular non-volatile storage elements relative to each other, each of the different groups including particular non-volatile storage elements with similar programmability.

6. (previously presented) The method according to claim 1, wherein:

said step of categorizing includes applying one or more non-zero source voltages to said particular non-volatile storage elements and, while applying said one or more non-zero source voltages, characterizing threshold voltages of said particular non-volatile storage elements by applying one or more positive voltages to control gates for said particular non-volatile storage elements and determining whether said particular non-volatile storage elements turn-on in order to determine whether said particular non-volatile storage elements have a threshold voltage greater than a negative voltage compare point.

7. (previously presented) The method according to claim 1, wherein:

said step of categorizing includes charging bit lines for said set of non-volatile storage elements, applying a control gate voltage and allowing said bit lines to discharge; and

said step of programming includes adjusting a subset of bit line voltages based on how said bit lines discharged.

8. (previously presented) The method according to claim 7, further comprising:

applying initial programming to said particular non-volatile storage elements prior to said step of programming, said step of categorizing is based on said step of applying initial programming.

9. (previously presented) The method according to claim 8, wherein:

said step of applying initial programming and said step of programming are performed using a common program voltage.

10. (previously presented) The method according to claim 9, wherein:

said common program voltage is applied via a common word line; and

said step of adjusting includes determining which of said particular non-volatile storage elements are slow to program, determining which of said particular non-volatile storage elements are fast to program and raising a voltage on bit lines for said particular non-volatile storage elements that are determined to be fast to program.

11. (previously presented) The method according to claim 8, wherein:

said step of applying initial programming is performed until at least one particular non-volatile storage element reaches a target threshold value; and

said step of categorizing is performed for particular non-volatile storage elements that did not yet reach said target threshold value.

12. (previously presented) The method according to claim 1, wherein:

said particular non-volatile storage elements are multi-state storage elements.

13. (previously presented) The method according to claim 1, wherein:

said particular non-volatile storage elements are multi-state NAND flash memory elements.

14. (previously presented) A system for programming non-volatile memory, comprising:

a set of non-volatile storage elements;

a set of control lines in communication with said set of non-volatile storage elements; and

a controlling circuit in communication with said control lines, said controlling circuit causes a categorizing of particular non-volatile storage elements in said set of non-volatile storage elements into three or more different groups, each particular non-volatile storage element being categorized into one of the different groups based on its detected behavior, and causes programming of each of said particular non-volatile storage elements using a different programming condition for each of the different groups.

15. (previously presented) The system according to claim 14, wherein:

said control lines includes a set of bit lines and a common word line;

said controlling circuit causes application of a program voltage on said common word line; and

said programming condition pertains to different bit line voltages.

16. (previously presented) The system according to claim 14, wherein:

said categorizing includes determining relative programming speeds of said particular non-volatile storage elements, each of the different groups including particular non-volatile storage elements with similar relative programming speeds.

17. (previously presented) The system according to claim 14, wherein:

said categorizing includes determining programmability of said particular non-volatile storage elements relative to each other, each of the different groups including particular non-volatile storage elements with similar programmability.

18. (previously presented) The system according to claim 14, wherein:

said categorizing includes applying a non-zero source voltage to said particular non-volatile storage elements and, while applying said non-zero source voltage, characterizing threshold voltages of said particular non-volatile storage elements by applying one or more positive voltages to control gates for said particular non-volatile storage elements and determining whether said particular non-volatile storage elements turn-on in order to determine whether said particular non-volatile storage elements have a threshold voltage greater than a compare point.

19. (previously presented) The system according to claim 14, wherein:

said categorizing includes charging bit lines for said particular non-volatile storage elements, applying a common control gate voltage and allowing said bit lines to discharge; and

said programming includes adjusting a subset of bit line voltages based on how said bit lines discharged.

20. (previously presented) The system according to claim 14, wherein:

said controller circuit causes initial programming to said particular non-volatile storage elements prior to said programming said particular non-volatile storage elements using a different programming condition, said categorizing is based on said initial programming.

21. (previously presented) The system according to claim 20, wherein:

said initial programming is performed until at least one of said particular non-volatile storage element reaches a target threshold value; and

said categorizing is performed for particular non-volatile storage elements that did not yet reach said target threshold value.

22. (previously presented) The system according to claim 20, wherein:

said initial programming is performed using a common word line voltage.

23. (previously presented) The system according to claim 14, wherein:

said particular non-volatile storage elements are multi-state storage elements.

24. (previously presented) The system according to claim 14, wherein:

said particular non-volatile storage elements are multi-state NAND flash memory elements.

25. (currently amended) A method for programming non-volatile memory, comprising:

applying initial programming to non-volatile storage elements until at least one non-volatile storage element reaches a target threshold value; and

~~subsequently~~ responsive to the at least one non-volatile storage element reaching said target threshold value, adjusting programming of at least a subset of non-volatile storage elements that have not reached said target threshold value based on behavior of said non-volatile storage elements that have not reached said target threshold value.

26. (previously presented) The method according to claim 25, further comprising:

characterizing said non-volatile storage elements that have not reached said target threshold value based on programmability, said step of adjusting is based on said step of characterizing.

27. (previously presented) The method according to claim 26, wherein:

said step of characterizing includes comparing a predetermined threshold voltage to threshold voltages for said non-volatile storage elements that have not reached said target threshold value.

28. (previously presented) The method according to claim 27, wherein:

said step of adjusting includes raising bit line voltages for non-volatile storage elements that have threshold voltages greater than said predetermined threshold voltage.

29. (previously presented) The method according to claim 25, wherein :

said step of applying initial programming to non-volatile storage elements includes applying a common program voltage to said non-volatile storage elements, said common program voltage increases at a first rate; and

said step of adjusting includes increasing a rate of increase of said common program voltage above said first rate.

30. (previously presented) The method according to claim 25, wherein :

said step of applying initial programming to non-volatile storage elements and said step of adjusting include applying a common program voltage to said non-volatile storage elements.

31. (previously presented) The method according to claim 25, wherein :

said step of applying initial programming to non-volatile storage elements and said step of adjusting include applying a common program voltage to control gates of said non-volatile storage elements.

32. (previously presented) The method according to claim 25, wherein:

said step of adjusting includes applying a non-zero source voltage to at least a subset of said non-volatile storage elements and comparing threshold voltages of said subset of non-volatile storage elements to a predetermined positive control gate value while applying said non-zero source voltage in order to determine programmability of said subset of non-volatile storage elements.

33. (previously presented) The method according to claim 25, wherein:

said step of adjusting includes charging bit lines for at least a subset of said non-volatile storage elements, applying a control gate voltage to said subset of said non-volatile storage elements and allowing said bit lines to discharge; and

said step of adjusting further includes adjusting a subset of said bit line voltages for programming based on how said bit lines discharged.

34. (previously presented) The method according to claim 25, wherein:

said non-volatile storage elements are multi-state storage elements.

35. (previously presented) The method according to claim 25, wherein:

said non-volatile storage elements are multi-state NAND flash memory elements.

36. (currently amended) A system for programming non-volatile memory, comprising:

a set of non-volatile storage elements;

control lines in communication with said set of non-volatile storage elements; and

a controlling circuit in communication with said control lines, said controlling circuit causes initial programming of said non-volatile storage elements until at least one non-volatile storage element reaches a target threshold value, and, responsive to the at least one non-volatile storage element reaching said target threshold value ~~subsequently~~, said controlling circuit causes adjustment of programming of at least a subset of non-volatile storage elements that have not

reached said target threshold value based on behavior of said non-volatile storage elements that have not reached said target threshold value.

37. (previously presented) The system according to claim 36, wherein:

said controlling circuit causes characterization of non-volatile storage elements that have not reached said target threshold value based on programmability, said adjustment of programming is based on said characterization.

38. (previously presented) The system according to claim 37, wherein:

said characterization includes comparing a predetermined threshold voltage to threshold voltages for said non-volatile storage elements that have not reached said target threshold, said predetermined threshold voltage is lower than said target threshold value.

39. (previously presented) The system according to claim 38, wherein:

said adjustment of programming includes raising bit line voltages for non-volatile storage elements that have threshold voltages greater than said predetermined threshold voltage.

40. (previously presented) The system according to claim 36, wherein:

said initial programming includes applying a common program voltage to said non-volatile storage elements, said common program voltage increases at a first rate; and

said adjustment of programming includes increasing a rate of increase of said common program voltage above said first rate.

41. (previously presented) The system according to claim 36, wherein:

said initial programming includes applying a common program voltage to said non-volatile storage elements.

42. (previously presented) The system according to claim 36, wherein:

said adjustment of programming includes applying a non-zero source voltage to at least a subset of said non-volatile storage elements and comparing threshold voltages of said subset of

non-volatile storage elements to a predetermined positive control gate value while applying said non-zero source voltage in order to determine programmability of said subset of non-volatile storage elements.

43. (previously presented) The system according to claim 36, wherein:

said adjustment of programming includes charging bit lines for at least a subset of said non-volatile storage elements, applying a control gate voltage to said subset of said non-volatile storage elements and allowing said bit lines to discharge; and

said adjustment of programming further includes adjusting a subset of said bit line voltages for programming based on how said bit lines discharged.

44. (previously presented) The system according to claim 36, wherein:

said non-volatile storage elements are multi-state storage elements.

45. (previously presented) The system according to claim 36, wherein:

said non-volatile storage elements are multi-state NAND flash memory elements.

46. (previously presented) A method for programming non-volatile memory, comprising:

applying an initial program voltage to a set of non-volatile storage elements;

applying one or more non-zero source voltages to said set of non-volatile storage elements after commencing said initial program voltage;

while applying said one or more non-zero source voltages, characterizing threshold voltages of said set of non-volatile storage elements by applying one or more positive voltages to control gates for said non-volatile storage elements and determining whether said non-volatile storage elements turn-on in order to determine whether said non-volatile storage elements have a threshold voltage greater than a compare point; and

adjusting a programming parameter of at least a subset of said non-volatile storage elements based on said step of characterizing.

47. (previously presented) The method according claim 46, wherein:

said compare point is a negative voltage.

48. (previously presented) The method according to claim 46, wherein:

said initial program voltage is applied via a common word line; and

said adjusting said programming parameter includes raising a voltage on one or more bit lines for said non-volatile storage elements.

49. (previously presented) A system for programming non-volatile memory, comprising:

a set of non-volatile storage elements;

control lines in communication with said set of non-volatile storage elements; and

a controlling circuit in communication with said control lines, said controlling circuit causes:

application of an initial program voltage to said set of non-volatile storage elements,

while applying one or more non-zero source voltages, characterization of threshold voltages of said set of non-volatile storage elements by applying a voltage to control gates for said non-volatile storage elements and determining whether said non-volatile storage elements turn-on in order to determine whether said non-volatile storage elements have a threshold voltage greater than a compare point; and

adjustment of control line voltages of at least a subset of said non-volatile storage elements based on said step of characterizing.

50. (previously presented) The system according to claim 49, wherein:

said control lines includes a set of bit lines and a common word line;

said initial program voltage is applied via said common word line; and

said adjustment of said control line voltages includes raising one or more bit line voltages.

51. (previously presented) A method for programming non-volatile memory, comprising:

applying an initial program voltage to a non-volatile storage element;

applying a verify voltage to a control gate for said of non-volatile storage element after commencing said applying of said initial program voltage;

charging a bit line for said of non-volatile storage element after commencing said applying of said initial program voltage;

allowing said bit line to discharge; and

adjusting a programming parameter of said non-volatile storage elements based on said bit line discharging.

52. (previously presented) The method according to claim 51, wherein:

said initial program voltage is applied via a common word line; and

said adjusting of said programming parameter includes raising a bit line voltage for said non-volatile storage element for subsequent programming.

53. (previously presented) The method according to claim 51, wherein:

said non-volatile storage element is a flash memory device.

54. (previously presented) A system for programming non-volatile memory, comprising:

a set of non-volatile storage elements;

a word line in communication with said set of non-volatile storage elements;

a set of bit lines in communication with said set of non-volatile storage elements; and

a controlling circuit in communication with said word line, said control lines, and said non-volatile storage elements, said controlling circuit causes:

application of an initial program voltage to said non-volatile storage elements,

application of a verify voltage at a word line for said of non-volatile storage elements after commencing said initial program voltage,

charging of bit lines for said of non-volatile storage elements after commencing said initial program voltage,

allowing of said bit lines to discharge,

adjustment of a programming parameter of at least a subset of said non-volatile storage elements based on said bit line discharging, and

completion of programming of said non-volatile storage elements using said adjusted programming parameter.

55. (previously presented) The system according to claim 54, wherein:

said initial program voltage is applied via said word line, said word line is common to all said non-volatile storage elements; and

said adjustment of said programming parameter includes raising one or more of said bit lines.

56. (previously presented) The system according to claim 54, wherein:

said program parameter is adjusted differently for different non-volatile storage elements.

57. (previously presented) The system according to claim 54, wherein:

said non-volatile storage elements are flash memory devices.